Abstract

[0057] A yield enhancement circuit substitutes a redundant sub-circuit for a faulty sub-circuit in an integrated circuit such as memory. The yield enhancement circuit has a plurality of fault indication devices, which is associated with one sub circuit of the integrated circuits such that one fault indication device is activated to generate a fault signal to express the existence of a fault within the faulty sub-circuit. Additionally selected adjacent fault indication devices generate the fault signal to express the existence of the fault within the faulty circuit. A fault detection device determines the existence of the faulty sub-circuit and transmits a redundancy implementation signal to a plurality of redundancy activation circuits. Each redundancy activation circuit selectively transfers input/output signals to a designated path dependent on the expression of the existence of a fault within the integrated circuit.